Low-Power Wireless ECG Acquisition and Classification System for Body Sensor Networks

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***Abstract*—A low-power biosignal acquisition and classification system for body sensor networks is proposed. The proposed system consists of three main parts: 1) a high-pass sigma delta modulator-based biosignal processor (BSP) for signal acquisition and digitization, 2) a low-power, super-regenerative on–off keying transceiver for short-range wireless transmission, and 3) a digital signal processor (DSP) for electrocardiogram (ECG) classification. The BSP and transmitter circuits, which are the body-end circuits, can be operated for over 80 days using two 605 mAH zinc–air batteries as the power supply; the power consumption is 586.5 μW. As for the radio frequency receiver and DSP, which are the receiving-end circuits that can be integrated in smartphones or personal computers, power consumption is less than 1 mW. With a wavelet transform-based digital signal processing circuit and a diagnosis control by cardiologists, the accuracy of beat detection and ECG classification are close to 99.44% and 97.25%, respectively. All chips are fabricated in TSMC 0.18-μm standard CMOS process.**

***Index Terms*—Body sensor network (BSN), electrocardiogram (ECG), high-pass sigma-delta modulator (HPSDM), super-regenerative on–off keying (OOK) transceiver, wavelet transform.**

I. Introduction

HEART disease has been the number one cause of death for a period of over 10 years [1]. Therefore, several medical devices have been developed to monitor the heart disease for healthcare. In recent years, body sensor network (BSN)-based applications or devices have become increasingly popular and widely accepted [2], [3]. People are now willing to use verified devices for biosignal acquisition, such as the electrocardiogram (ECG) or the electroencephalogram, because these devices can help in monitoring patient health in real time [4], [5]. With the development of networks, collected health information can be sent to the cloud server of the nearest clinic or hospital. Doctors can then provide patients with medical advice. In other words, BSN-based devices or applications can help both patients and doctors in daily health monitoring.

Several BSN-based systems have been proposed. Baek *et al.* proposed a smart health monitoring chair that allows the non-invasive measurement of biosignals [6]. This chair is suitable for home care systems without wearing anything if the continuous tracking ECG signal is not required. Vuorela *et al.* proposed a portable physiological signal recorder [7] that is quite convenient for patients; however, signals are recorded in the recorder's memory and cannot be observed in real time. Yang *et al.* demonstrated a low-power, biopatch prototype with flexible electrodes [8]. This prototype is considerably suitable for portable health monitoring systems, but it lacks a wireless communication feature. Tsai *et al.* proposed a complete BSN system for ECG measurement [9], but its power consumption is relatively high, thus making it inappropriate for long-term use. Yan *et al.* demonstrated a wearable cardiac monitoring system with 25 electrodes [10]. The system features a complete system-on-chip (SOC) system and the ability to wirelessly transmit ECG signals. However, the location and the transmission distance are limited because of the use of inductive coupling. Therefore, an ideal BSN system must be applicable in the long term and is convenient; it must also provide on-time monitoring and allow wireless communication.

This study proposes a biosignal acquisition and classification system. This system features low-power consumption, wireless transmission, and on-time monitoring. This system can be used in wearable wireless ECG acquisition systems and consists of three main blocks: a biosignal processor (BSP), an on–off keying (OOK) transceiver, and a digital signal processor (DSP). The BSP circuits are composed of a chopper-based continuous-time amplifier (CBCTA) and one high-pass sigma-delta modulator (HPSDM). These two circuits reduce front-end circuit complexity to save power consumption while maintaining a high resolution (>12 bits). Transceivers are always the most power-hungry devices; therefore, the super-regenerative transceiver is employed because of its low power and low circuit complexity. For real-time detection and ECG classification, a DSP circuit with wavelet transform is implemented to achieve these features. Therefore, the proposed system can provide a low-power SOC solution for wireless ECG acquisition and classification systems.

This paper is organized as follows. Section II describes the proposed system. Section III presents the circuit implementations. Section IV discusses the measurement results. Section V concludes the paper.

Manuscript received July 5, 2013; revised November 7, 2013 and February 8, 2014; accepted February 24, 2014. Date of publication March 11, 2014; date of current version December 30, 2014. This work was supported in part by the Chip Implementation Center and the National Science Council (NSC) of Taiwan under Grants NSC102–2221-E-006-289-MY3, NSC102-2220-E-006-020, and NSC 101-3113-P-006-025.

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Digital Object Identifier 10.1109/JBHI.2014.2310354

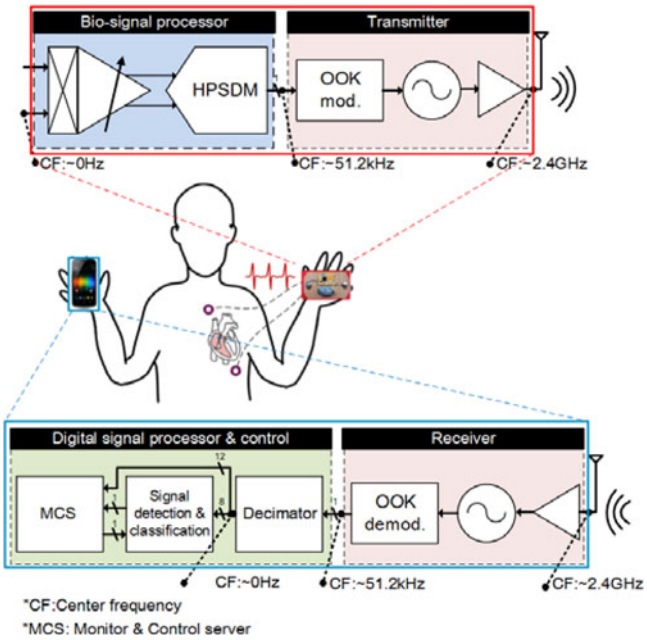

Fig. 1. Block diagrams of the proposed low-power wireless biosignal acquisition and classification system.

II. ECG Acquisition and Classification System

The proposed system is shown in Fig. 1. The biosignals are sensed by the BSP circuits and converted to digital signals. The data are then sent out by the transmitter. The signals are received and processed by the receiver and DSP, respectively. The body-end circuits and receiving-end circuits are the two main parts of the system. The design objectives of the body-end circuits, which are composed of the BSP and the transmitter, are 1) low power consumption for long-term usage and 2) acquisition resolution that is high enough for ECG signal classification. Given these two objectives, the body-end circuits should have low circuit complexity and require an appropriate architecture for the transceiver to achieve the demand for low-power consumption. For the receiving-end circuits, the major objectives are 1) recovering the radio frequency (RF) signal and 2) recovering the biosignal classification. However, the receiving-end circuits can be integrated into a monitoring and control service (MCS), which can come in the form of a smartphone or a personal computer. Unlike body-end circuits, recovering-end circuits do not urgently require low-power consumption, as these devices can share the same power source. The following sections describe the major concerns of the proposed system.

A. Biosignal Processor

The proposed BSP circuits, which are composed of only one CBCTA and one HPSDM [11], and the block diagrams are shown in Figs. 2(a) and 5(a), respectively. First, the frequency of biosignals is shifted to a high frequency by the chopper to avoid the injection of low-frequency noises such as flicker noise. Second, the frequency-shifted signals are amplified by the continuous-time feedback amplifier until the adequate voltage level for data conversion is achieved. Third, the amplified

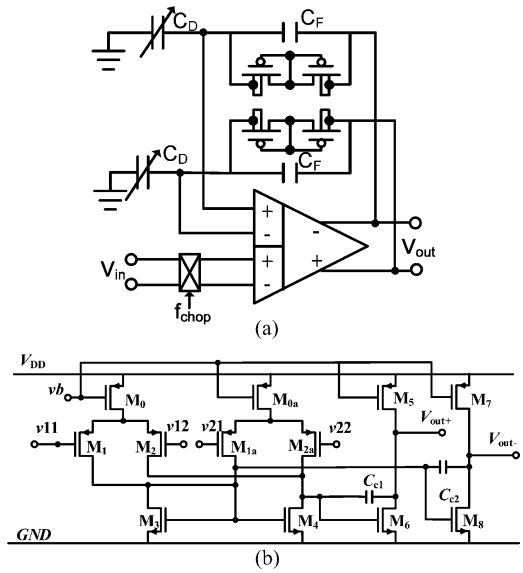

Fig. 2. (a) Chopper-based continuous time amplifier. (b) Circuits of the DDA.

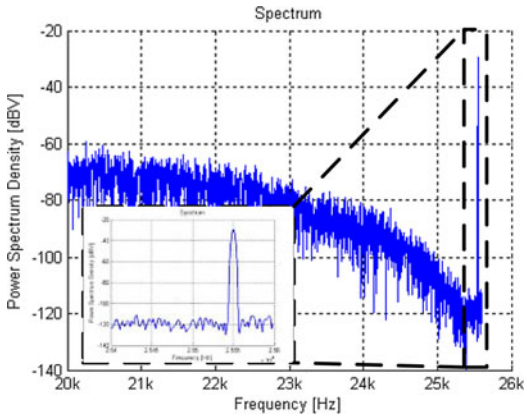

Fig. 3. Output spectrum of the HPSDM.

signal is delivered directly to the HPSDM without shifting the frequency back to the direct current (DC). The signal is modulated with quantization noise by the HPSDM. Finally, the signal with 1-bit stream output passes directly through the transmitter without the serial-to-parallel circuit. As the biosignals are oversampled and modulated with quantization noise by the HPSDM, the modulated signals are similar to random signals because the low-frequency noise is modulated in the spectrum as shown in Fig. 3. These random signals can go against channel noise during wireless communication. They can even avoid encryption by the encoder and tolerate the high bit error rate (BER) of RF transmission to save the power. Fig. 4 illustrates the BER versus signal-to-noise ratio (SNR) of the received data at the decimator output based on the interception of 50 000-point data from a 1-bit stream output of the HPSDM. The ideal peak SNR without channel noise is 59 dB, with a 50-Hz and 100-$mV_{\text{peak-to-peak}}$ sinusoidal input. Additive white Gaussian noise is included in the channel model to evaluate BER versus SNR at the decimator output. If the SNR of BSP is 60 dB, the BER of 10^{-3} can be maintained even if the received data at the decimator output have

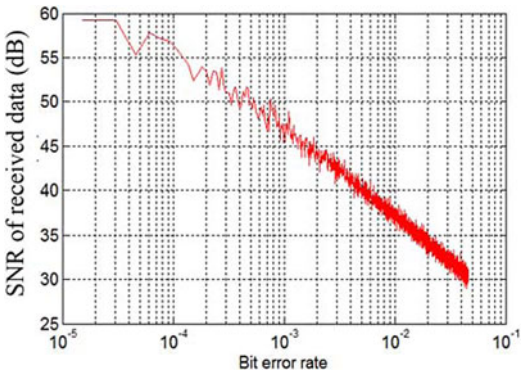

Fig. 4. BER versus SNR of received data.

SNR of 48 dB without any encoder or error debugger. Moreover, a BER of less than 10^{-4} can be achieved if the received SNR at the decimator output is higher than 55 dB.

The proposed BSP circuits differ from conventional analog front-end circuits and have several advantages. 1) They have simplified circuit complexity but maintain a high resolution. 2) They do not require the antialiasing filter, which always dominates the system performance. 3) Demand for an additional digital circuit, such as an encoder for encryption or a parallel-to-serial circuit behind an analog-to-digital converter (ADC) for the 1-bit stream transmission, does not exist.

B. Super-Regenerative OOK Transceiver

Several conditions should be considered with regard to wireless transmission in the BSNs. These conditions include the transmission frequency, safety, transmission distance, transmission power, data rate, and the power consumption of the transceiver. First, the absorption rates of the human body, which are related to safety, decrease with the high frequency ranging from 300 MHz to 3 GHz in the frequency domain [12]. Second, the proposed system may be integrated into other devices, such as smartphones or personal computers. Thus, the transmission frequency should be referred to the ISM band to be universally compatible. However, the use of a 433.92-MHz frequency is limited in Region I, as is the use of a 915-MHz frequency in Region II [13]. Therefore, a frequency of 2.4 GHz is the better choice compared with other frequency bands [13].

Safety, especially the limitation imposed by the maximum permissible exposure (MPE) is the biggest concern in BSNs [14], [15]. The MPE is derived from the specific absorption rate (SAR), which refers to the RF energy being absorbed by the body. When the body absorbs RF energy, it will be heated. If the temperature rises to more than just 1°C, adverse health effects may occur. According to [16], the sum of the products of exposure levels and the allowed time for exposure must be less than or equal to the product of the limited MPE regulation and its corresponding average time. Table I indicates the required maximum MPE as reported by IEEE and ICNIRP.

The power spectrum density can be represented as

$$\text{Power Density}(S) = \frac{P_t G_t}{4\pi R^2} \quad (1)$$

TABLE I
LIMITS FOR THE MPE

	Power density (W m^{-2})	
	Controlled exposure (6 minutes average)	Uncontrolled exposure (6 minutes average)
IEEE [14]	80	50
ICNIRP[15]	50	10

TABLE II
SPECIFICATION COMPARISONS AMONG DIFFERENT TRANSCEIVER ARCHITECTURES

Architecture	Sensitivity	Data Rate	Circuit complexity	Power consumption
Super Heterodyne	High	High	High	High
Direct Conversion	Medium	Medium	Low	Medium
Low IF	Medium	Medium	Medium	Medium
Super Regeneration	Low	Low	Low	Low

where P_t is the transmitting power, G_t is the power gain of the antenna, and R is the distance to the center of radiation of the antenna. The proposed system is applied in BSNs, and the distance between the body-end device and the receiving device is assumed to be 1 m. If the maximum transmitting power is -10 dBm, then the power gain of the antenna is 0 dBi, and the body-end device, including the BSP and transmitter, is near the body. Furthermore, the power density is 0.08 W/m^2 within the distance of 1 cm and 0.02 W/m^2 within the distance of 2 cm. These values are less than the limitation of the MPE (see Table I). Therefore, the maximum output power of the transmitter can be designed under -10 dBm. Moreover, the transfer of energy via the Friis transmission equation can be adopted to estimate the energy loss in the air [17]. The loss under a distance of 1 m is about 40 dB. Therefore, the required sensitivity of the receiver should be less than -50 dBm.

Several transceiver architectures can be employed [18], [19] to achieve the required wireless biosignal transmission. The general specification comparisons of different transceiver architectures are shown in Table II. The characteristics of a wireless ECG acquisition system are as follows: short-range transmission, low-power consumption demand, and low data rate. Super regeneration [19] is preferred in the proposed system.

C. Digital Signal Processor

The DSP has two main functions. One is demodulating and shifting the frequency back to the baseband, and the other is classifying the ECG signals [20]. As a result of their modulation with quantization noise to combat transmission error, the signals cannot be displayed directly by the MCS. Although the original signals are frequency shifted to a high frequency, modulated, and influenced by transmission error, they can still be recovered correctly by the DSP and remain in the required resolution.

Wavelet theory is widely adopted for the feature extraction and classification of biosignals because of its scalable coefficient and time–frequency representation. The discrete wavelet transform (DWT) is commonly used because of its fast computation,

and because it is suitable for implementation with digital circuits [21]. For ECG classification, the ECG signal information from MIT-BIT database [22] can be prestored in the DSP memory database and compared with the analyzed data. The DSP searches the database for the most similar ECG signal and export the classification results. The database can also be updated from the MCS, which is wirelessly controlled by cardiologists.

III. Circuit Implementation

A. Chopper-Based Continuous Time Feedback Amplifier

In biosignal acquisition or processing, noise reduction is always a big challenge, and it cannot be eliminated completely. The most common intrinsic noises are thermal noise and flicker noise [23]. Thermal noise can be suppressed by increasing the transconductance of input transistors. Flicker noise can be avoided using circuit techniques, such as combining the amplifier and the chopper [23]. Fig. 2 shows the CBTCA and the detailed circuit schematic of the difference differential amplifier (DDA). According to [24], this architecture can be used not only as an amplifier but also as a bandpass filter. The close-loop gain can be determined by the ratio of C_D and C_F. The bandwidth can be designed based on the combination of C_D, C_F, and feedback resistor R_F. The transfer function of the CBTCA and its parameters are as follows:

$$H(s) \approx \frac{G_{m1}[s + \frac{1}{R_F(C_F+C_D)}]}{C_C s^2 + \frac{G_{m2}C_F}{C_F+C_D}s + \frac{G_{m2}}{R_F(C_F+C_D)}} \tag{2}$$

$$\text{Mid-band gain} = \frac{G_{m1}(C_F + C_D)}{G_{m2}C_F} \tag{3}$$

$$f_{\text{zero}} = \frac{1}{R_F(C_F + C_D)} \tag{4}$$

$$f_{\text{high}-3\text{dB}} = \frac{G_{m2}C_f}{(C_f + C_d)C_c} \tag{5}$$

$$f_{\text{low}-3\text{dB}} = \frac{G_{m2}C_F}{C_C(C_F + C_D)}. \tag{6}$$

For the wide biosignal range and gain-tunable application, the mid-band gain can be 20, 24, or 28 dB, along with three sets of C_D capacitor. The transistor-based pseudoresistors not only determine the zero/pole of the $H(s)$ but also supply the required dc voltage of the amplifier's input on the feedback path.

B. High-Pass Sigma-Delta Modulator

Sigma-delta modulator (SDM) is widely used in low-frequency applications because of its high resolution. In addition, the central frequency can be modified with different applications, such as the low-pass SDM (LPSDM) or the bandpass SDM. Given the shift of the biosignal to a high frequency by the CBCTA, a HPSDM is chosen as an ADC in the biosignal processing circuit. Fig. 5(a) shows the system architecture of the SDM. Similar to the design technique of the LPSDM, the high-pass transfer function can be obtained from a low-pass transfer function with $z \to -z$, shifting its central frequency from 0 to $f_s/2$. Its stability is considered to be the same as that

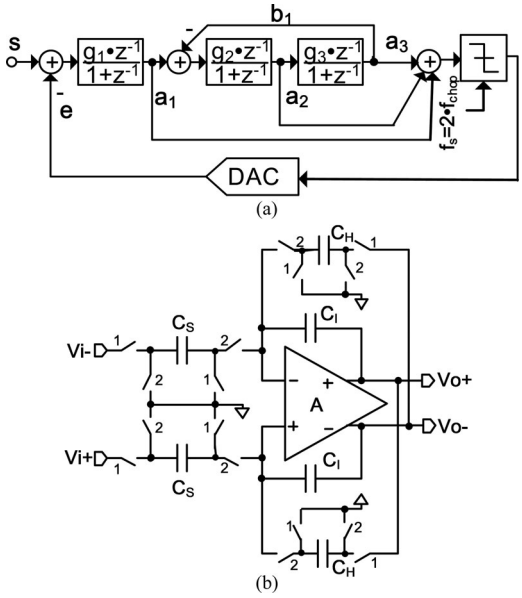

Fig. 5. (a) Third 1-b HPSDM with feed-forward topology. (b) Schematic of first-order high-pass integrator.

of the LPSDM design [25]. The relative transfer function at the summation point of a1, a2, and a3 are derived as [see Fig. 5(a)]

$$a_1 = (s - e)\frac{g_1 z^{-1}}{1 + z^{-1}} \tag{7}$$

$$a_2 = (s - e)\frac{g_2 g_1 \left(1 + z^{-1}\right) z^{-2}}{\left(1 + z^{-1}\right)^3 + b_1 g_2 g_3 \left(1 + z^{-1}\right) z^{-1}} \tag{8}$$

$$a_3 = (s - e)\frac{g_3 g_2 g_1 z^{-3}}{\left(1 + z^{-1}\right)^3 + b_1 g_2 g_3 \left(1 + z^{-1}\right) z^{-2}}. \tag{9}$$

The first-order high-pass integrator can be realized by switched-capacitor circuits [see Fig. 5(b)], and its transfer function can be expressed as [26]

$$H(z) = \frac{C_S}{C_I} \cdot \frac{z^{-1}}{1 + (\frac{C_H}{C_I} - 1)z^{-1}} \tag{10}$$

where $C_H = 2C_I$.

Moreover, the nonideal effects such as thermal noise, finite gain and finite bandwidth of OPAMP, clock jitter, and coefficient variation have been analyzed in the implementation of this HPSDM [27]. Therefore, the minimum specification requirements of the OPAMP can be obtained, and the power consumption of HPSDM can be minimized.

C. Super-Regenerative OOK Transceiver

Fig. 6(a) shows the transmitter that is composed of a complementary cross-coupled pair voltage-controlled oscillator (VCO) and a self-biasing buffer with OOK modulation. The OOK modulator that is controlled by input data can be used with two simple NMOS components: one provides negative resistance for the VCO, and the other controls the current path of the output buffer.

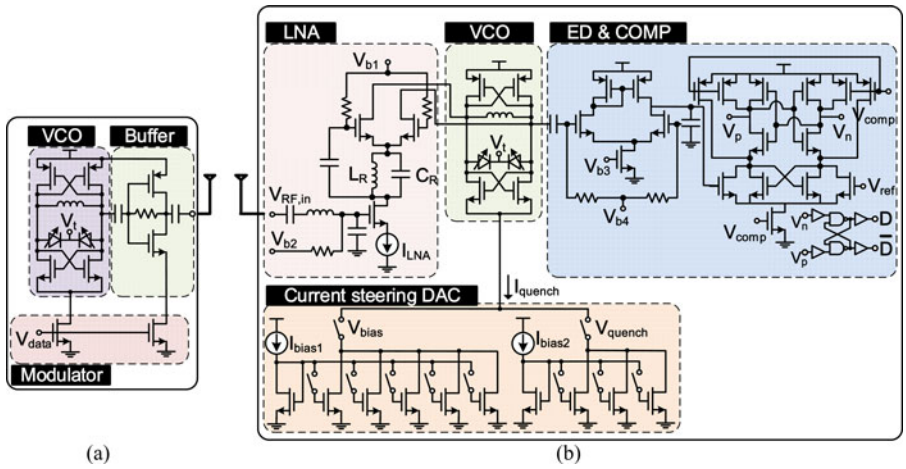

Fig. 6. Circuit diagram of the proposed super-regenerative transceiver. (a) Transmitter. (b) Receiver.

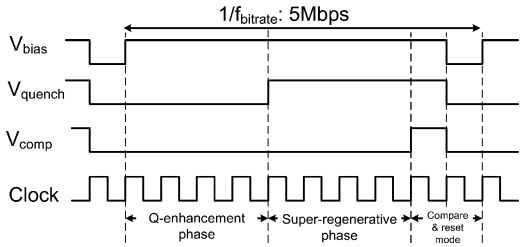

Fig. 7. Control signals of the Q-enhancement technology on the receiver.

The proposed transceiver should meet communication standards in view of safety and commercial concerns. An ISO 18000-4 [28] is adopted in our design as the reference of BSNs under the 2.45-GHz carrier frequency and OOK modulation. According to the standard that is defined by the rise and fall times of the modulation signal, the maximum time is $0.1/f_{\mathrm{bitrate}}$, where f_{bitrate} is the frequency of the bit rate. Therefore, the rise and fall times for the maximum data rate of 5 Mbps should be less than 20 ns to meet the standard. As the rise and fall times are determined by the bias current of the VCO, the current of 400 μA can be high enough to meet these specifications. Moreover, a class-AB amplifier with 400 μA is used as the output buffer in the transmitter because its linearity is more moderate than that of the class-A and class-B amplifiers, and because it can be operated with self-bias.

The frequency selectivity of OOK receivers can be improved with Q-enhancement technology [19]. The proposed receiver with Q-enhancement technology [see Fig. 6(b)] is composed of an LNA, a VCO with digital-to-analog converter (DAC)-controlled current source, an envelope detector, and a comparator. Given the requirement of these control signals, the waveform of the control signal can be arranged, as shown in Fig. 7. The input data are processed in four phases: 1) Q-enhancement phase, 2) super-regenerative phase, 3) comparison phase, and 4) reset phase. In the Q-enhancement phase, the receiver acts as a bandpass filter and reserves the target data on the bandwidth. In the super-regenerative phase, the VCO is oscillated because the bias current (I_{quench}) that is controlled by the current steering DAC is turned ON. Furthermore, the oscillated amplitude will be processed by envelop detector and comparator in comparison phase to extract the received data.

TABLE III
SPECIFICATIONS OF EACH STAGE IN THE PROPOSED DECIMATOR

Parameters	Comb. filter	Compensation filter	FIR filter I	FIR filter II
Sampling frequency (Hz)	51200	1600	1600	800
Decimation rate	32	1	2	2
Passband edge (Hz)	N.A.	180	180	180
Stopband edge (Hz)	N.A.	200	620	220
Passband ripple (dB)	N.A.	< 0.01	< 0.01	< 0.01
Stopband attenuation (dB)	N.A.	$\geqq 60$	$\geqq 60$	$\geqq 60$
Output sampling frequency	1600	1600	800	400

D. Decimation Filter

The signal should be demodulated and downsampled to the baseband in the receiver because the ECG signal has been digitized and modulated by the HPSDM on the body-end circuits. First, the signal can be reduced from 51.2 kHz to DC with one XOR gate. Second, the out-of-band noise can be eliminated by the digital low-pass filter. Afterward, the frequency of the digital filter output is downsampled to 400 Hz (Nyquist sampling frequency) [29].

The decimation filter is implemented in the following four stages to balance hardware and complexity: one combination filter, one compensation filter, and two FIR filters. Considering the high frequency of the first stage of the decimation filter, comb filters, which have large decimation ratio and lower circuit complexity than the FIR filter, are preferred in the first stage [30]. Two FIR filters with a decimation ratio of 2 can be used in the remaining stages. The details are shown in Table III. After demodulation, the signal can be directly displayed on the smartphone and can even be analyzed by the other DSP processor. However, the word length of the decimator should also

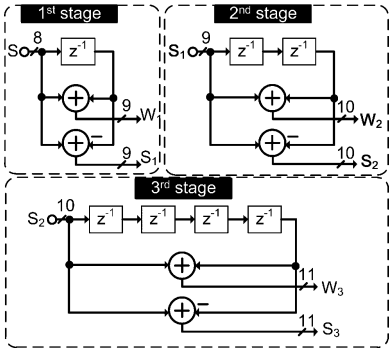

Fig. 8. Block diagram of the previous three stages of the Haar wavelet.

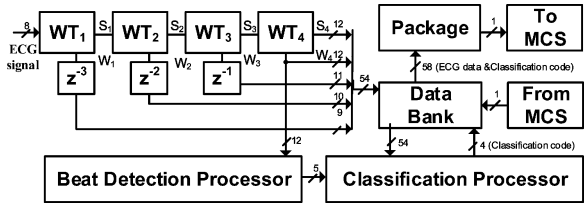

Fig. 9. Block diagram of the wavelet transform processor.

be considered, and the balance between precision and hardware cost should be maintained. The target SNR of the BSP is about 72 dB, and the decimator should eliminate the out-of-band noise and recover the SNR specification. According to the simulation results from MATLAB, the 18-bit word length is used.

E. Wavelet Transform Processor

The DWT function is defined in (11)–(12) [31], where $S(n)$ is the input signal, $\phi_{j0,k}(k)$ is the impulse response of the scaling function (low-pass filter), $\psi_j, k(k)$ is the impulse response of the wavelet function (high-pass filter), j is the scale of the wavelet decomposition, j_0 is the scale 1 wavelet transform, k is the sample points, and M is the dilation which is equal to 1 in this paper

$$W_{\phi_{j_0,k}}(n) = \frac{1}{\sqrt{M}} \sum_k \phi_{j_0,k}(k) S(n-k) \tag{11}$$

$$W_{\psi_{j,k}}(n) = \frac{1}{\sqrt{M}} \sum_k \psi_{j,k}(k) S(n-k). \tag{12}$$

According to the tradeoff between the hardware cost and power consumption, the simple Haar wavelet can be adopted to implement the required circuits. The transfer functions of scales are as follows:

$$W_i = H_{\phi i}(z) = 1 + z^{-2^{i-1}} \tag{13}$$

$$S_i = H_{\psi i}(z) = 1 - z^{-2^{i-1}} \tag{14}$$

where i is the scale numbers as shown in Figs. 8 and 9. According to the impulse response of the Haar wavelet, these functions can be implemented with a simple FIR filter (see Fig. 8). A fourth-order Haar wavelet-based DWT is implemented in the receiver to detect and classify the signal beat.

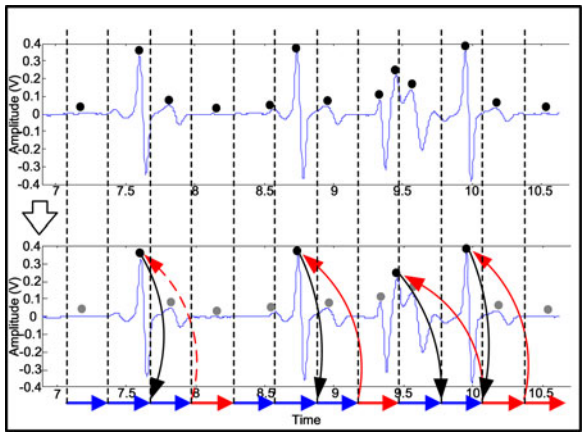

Fig. 10. Timing response of the R-wave detection algorithm.

Fig. 9 shows the block diagram of the wavelet transform processor. The digitized ECG signal at the decimator output is fed into the fourth-order DWT processor, and the coefficients of $[W_1, W_2, W_3, W_4, S_4]$ can be extracted from the ECG signals. The W_4 coefficient is adopted in the beat detection algorithm to evaluate the frequency location of the ECG beats. As the maximum human heart rate does not exceed 220 beats/min (BPM) [32], the beat detection window can be defined as 32 points with a 120-Hz sampling rate to cover the maximum BPM occurrence. The maximum peak can be easily detected by comparing the local peaks within 32 points of the detection section.

The proposed beat detection algorithm is different from the conventional beat detection algorithms [33] with a sixth-order DWT. To reduce circuit complexity, the proposed algorithm is based on the detection of W_4 coefficient only from the wavelet transform. The baseline always changes because of the motion artifact and respiration, but the effect can be eliminated in W_4 coefficients to accurately recover the original ECG. Therefore, the W_4 coefficient without the low-frequency component is highly suitable for beat detection and for the simplification of the detection algorithm. As shown in Fig. 10 and as mentioned in the previous paragraph, each section has 32 points. The normal beat can be detected within the four sections. The DSP function of beat detection is designed for the following actions. First, the DSP circuit finds the local maximum value in each section. Second, the local maximum value is compared with the nearest four sections, and the maximum value that is found is considered as the beat. However, if the difference in voltage is relatively small within the four sections (e.g., within one-fourth of the peak value), the two signals are assumed as beats. Therefore, the beat can be detected with this simplified algorithm.

For the ECG classification, the initial classification is recommended by the cardiologist to achieve precise findings. The cardiologist reads the ECG signal on the MCS and checks if the signal indicates a normal beat or other symptoms. For the ECG classification algorithm, the classification data of symptoms information, with a maximum of eight symptoms, are diagnosed on the MCS by cardiologists. The cardiologists then

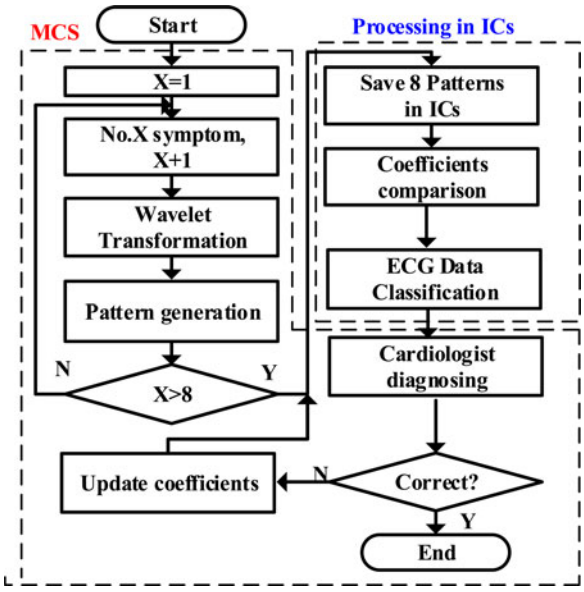

Fig. 11. Classification procedure between the MCS and the wavelet transform circuits.

use the results on the screen to program the weight of the wavelet coefficients (see Fig. 11). These new coefficients are stored on the data bank of the wavelet transform processor and can be updated using the MCS. This new feature with a programmable DSP can help cardiologists in customizing the proposed device to satisfy the needs of different cardiac patients.

IV. Measurement Results

Three chips in the proposed system were implemented separately with TSMC 0.18-μm standard process for system verification. In accordance with the practical usage scenario, the first chip, including the BSP and the transmitter, is implemented as the body-end circuit. The second chip, with the receiver and the decimator, is used to recover the ECG signal. The third chip with wavelet transform is designed to test the ECG signal classification. The microphotographs of these three chips are shown in Fig. 12. Their core areas are 1.52×1.55, 1.28×2.04, and 1.57×1.57 mm^2, respectively. The measurement results are based on the three parts of the system, namely, the BSP circuit, transceiver, and DSP circuit. The integrated platform is also adopted to reveal the scenario of the proposed system.

A. Biosignal Processing Circuit

Fig. 13 shows the two-tone test of the BSP circuit, with an input signal amplitude of 2.5 mV and frequencies of 70 and 100 Hz to measure the third- and fifth-harmonic distortions, it reveals the peak SFDR of about 68 dB. Lead II of the ECG signals is acquired by a Wilson circuit [32] and then fed into the BSP circuit. In Fig. 14, most of the ECG signals are located at the low-frequency bands. Through the BSP circuits, the amplitude of ECG signals is enhanced, and their frequencies are shifted to a high-frequency band. The power noises with frequencies of 60 and 180 Hz that are received by the human body are also

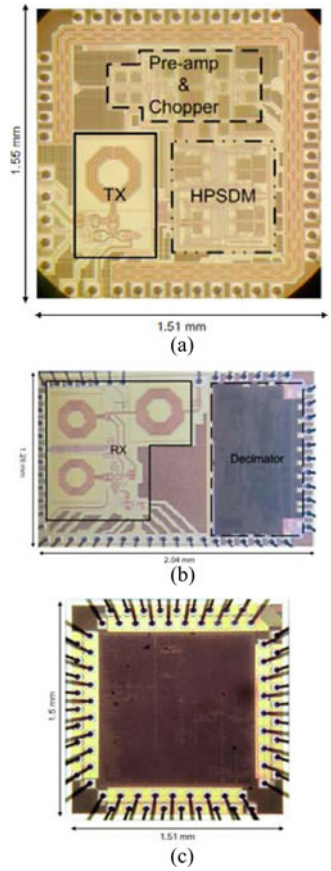

Fig. 12. Microphotographs of the proposed BSN system: (a) BSP and transmitter, (b) receiver and decimator, and (c) DSP circuits.

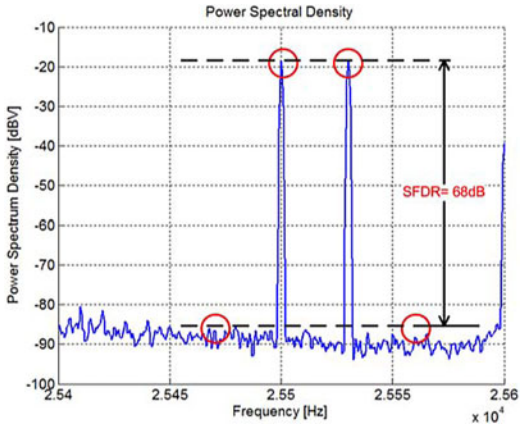

Fig. 13. Output spectrum of the BSP with two-tone test.

amplified and frequency shifted by the BSP circuit; they should be eliminated by the digital processor on the MCS.

B. Transceiver

According to the different controlled voltages, the output frequency of the transmitter could be adjusted to a specific frequency (see Fig. 15) for wireless communication. The measured tuning range of 2.17 to 2.59 GHz meets the ISO 18000-4 standard [28]. Fig. 16 shows the maximum output energy of

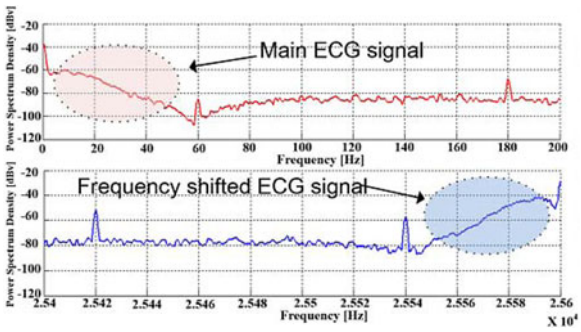

Fig. 14. Measured ECG signal (before and after frequency shifted).

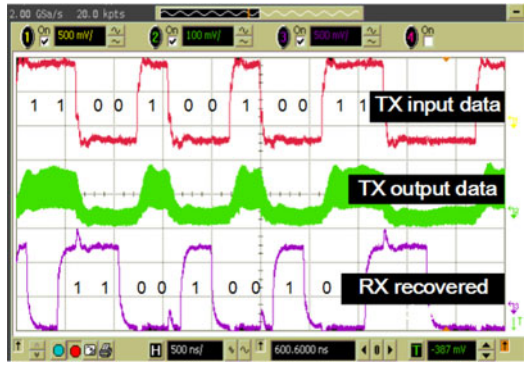

Fig. 17. Measured waveforms of the transmitter and receiver.

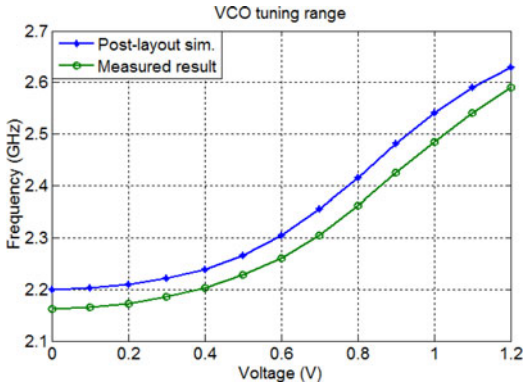

Fig. 15. Tuning range of the transmitter VCO (postlayout simulation versus measured results).

Fig. 18. Measured classified ECG data (screenshot of the smartphone).

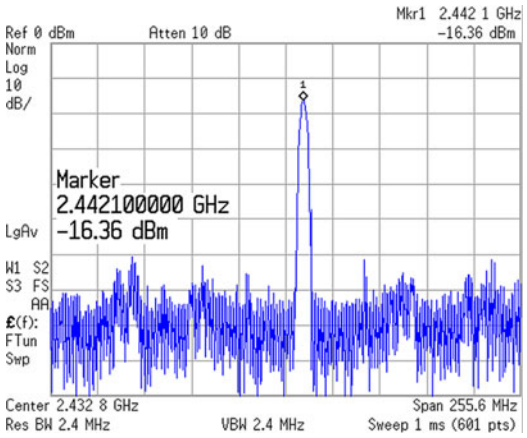

Fig. 16. Output spectrum of the transmitter with the maximum output power of −16.36 dBm.

−16.36 dBm. Fig. 17 shows the transient response of the transceiver with duty cycle of 400 ns and reveals that the transmitted signal can be correctly recovered on the receiver.

C. Digital Signal Processing Circuit

The MIT-BIH database [22] has been applied in the classification test of the wavelet transform circuit. To test the correctness of the classification function for simplicity, several ECG data with disease symptoms, referred to as the MIT-BIH database, were combined into one data stream as the input of the wavelet transform circuit. An Altera cyclone IV FPGA, with an additional Bluetooth module, was applied for the classification function to achieve a distinct display. With Bluetooth and the self-developed APP program, the classification results can be displayed on the smartphone, as shown in Fig. 18, where the annotation codes represent the ECG waveform with different features. The annotation codes are defined in [22]. The codes include "N," which represents the normal beat, "a," which represents the aberrated atrial premature beat, and "V," which represents premature ventricular contraction.

D. Integrated Platform

Fig. 19 shows the platform of the proposed wireless ECG acquisition and classification system. The Lead II ECG signal is acquired and transmitted by the body-end circuit. The signal is then recovered and classified by the receiving-end circuit under 10-cm distance in the air only because of poor reliability between the RF transmitter and receiver circuits. The recovered signal and the classified results are then sent to the smartphone via Bluetooth technology. The measured ECG signals as displayed on the smart phone are shown in Fig. 20. The comparison and the specifications of the proposed BSN system are illustrated in the Tables IV and V [11], respectively. As shown in Table V, the total power consumption including an analog

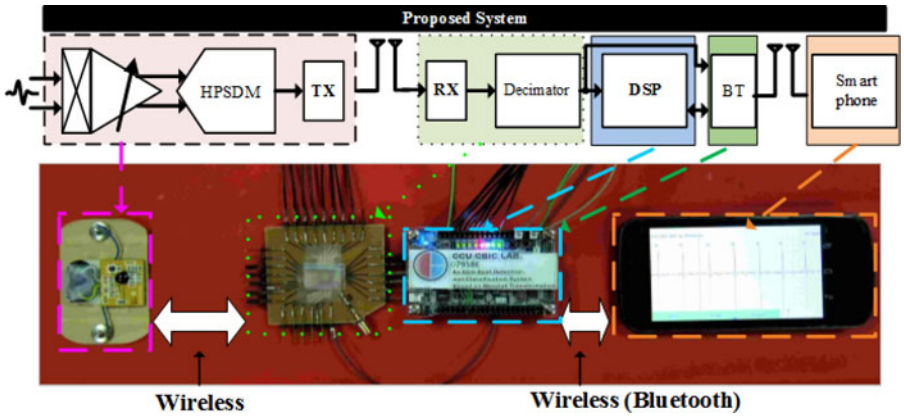

Fig. 19. Measurement environment of the proposed system.

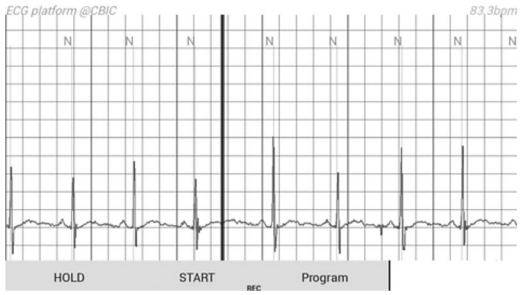

Fig. 20. Measured ECG Lead II data (screenshot of the smartphone).

TABLE IV
PERFORMANCE COMPARISON WITH STATE OF ART

	This Work	[35]	[36]	[10]	[37]
Tech(um)	0.18	0.13	0.13	0.18	0.065
Power consumption	1.5 mW	19 uW	17 uW	2.4 mW	N/A
Analog Front End					
Bandwidth(Hz)	200	320	N/A	250	292
Gain (dB)	20 - 28	40 - 78	36 - 44	18 – 40	45 - 60
ADC architecture	12-bit SDM	8-bit SAR	8-bit SAR	10-bit ADC	10-bit SAR
Wireless transmission					
TX output power	-16.36 dBm	-18.5 dBm	-18 dBm	-6 dBm	-13 dBm
TX energy per bit	0.1 nJ/bit	0.8 nJ/bit	4 nJ/bit	2.8 nJ/bit	0.15 nJ/bit
RX energy per bit	0.088 nJ/bit	No RX	3.8 nJ/bit	N/A	No RX
Features					
QRS detection	✓	×	×	×	×
Biosignal Classification	✓	×	×	×	×
Impedance Variance	×	×	×	✓	×

front-end, a transceiver, and a DSP, is 1.5 mW. The proposed system provides not only the wireless biosignal acquisition but also the classification. The resolution of this work is higher than that of previous works. And the pie-chart of power consumption is shown in Fig. 21 also for describing the distribution of the subcircuit power.

TABLE V
SPECIFICATIONS SUMMARY OF THE PROPOSED SYSTEM

General specifications		
Technology	TSMC 0.18 µm 1P6M standard CMOS process	
Chip Area	1.52×1.55 mm^2 (AFE +TX) 1.28×2.04 mm^2 (RX + decimator) 1.57×1.57 mm^2 (detection and classification)	
Carrier frequency	2.4 GHz	
Supply voltage	1.2 V	
AFE+TX		
Chopper-based amplifier	Chopper frequency	25.6 kHz
	Mid-band gain	20/24/28 dB
	Power consumption	17 µW
HPSDM	Bandwidth	200 Hz
	Sampling frequency	51.2 kHz
	Resolution	10 bits
	Power consumption	37.5 µW
Transmitter	VCO tuning range	2.17 GHz to 2.59 GHz
	Duty cycle	400 ns
	Output power	-16.36 dBm
	Energy per bit	106 pJ/bit
	Power consumption (50% 1's period)	532 µW
RX + decimator		
Receiver	Power consumption	440 µW
	Max. data rate	5 Mbps
	Energy per bit	88 pJ/bit
Decimator	Word length	18 bits
	sampling frequency	51.2 kHz
	Power consumption	454 µW
detection and classification		
Signal detection and classification	Operation frequency	120 Hz
	Available symptoms	8 Kinds
	Power consumption	5.967 µW

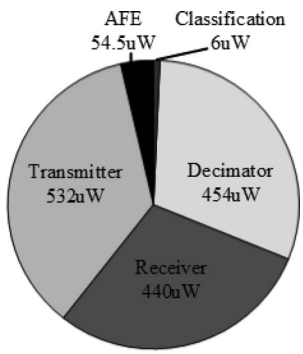

Fig. 21. Pie-chart of the power consumption of subcircuits.

V. Conclusion and Discussion

This study proposes a biosignal acquisition and classification system with wireless telemetry for BSN. Three chips, namely, a body-end chip, a receiving-end chip, and a classification chip, are implemented in TSMC 0.18-μm standard CMOS process. The total power consumption of the body-end circuit is 586.5 μW, with only 1.2 V of supply voltage. Fitted with two 605-mAh PR44 zinc-air batteries, the wearable wireless ECG acquisition system, which includes a digitizer and a transmitter, can be operated for over 80 days. The accuracy in terms of beat detection and classification are 99.44% and 97.25%, respectively. These results indicate that the proposed system can correctly diagnose heart disease based on the MIT-BIH arrhythmia database. The symptoms, which can be suggested and controlled by cardiologists on the MCS, can be used to update the coefficients of wavelet transform on the DSP chip. Therefore, the device can assist the cardiologists in diagnosing their patients, and the customized device can be used by patients as their "virtual cardiologist."

Most of the main functions of the proposed system have been tested and verified. However, this system still needs further improvement, particularly in the synthesizer design of the transceiver for multichannel biosignal acquisition, the feedback control for the body-end chip, the integration of the receiver and the DSP circuit in a single receiving-end chip, and the combination of the receiving-end chip and the smartphone. The new functions and further integration will be studied in the future to complete the personal care device for BSNs.

Acknowledgment

The authors would like to thank the Chip Implementation Center in Taiwan for its technical support as well as M. Y. Huang and Y. H. Cheng of the Communication and Biologic Integrated Circuit Laboratory for their assistance in this study.

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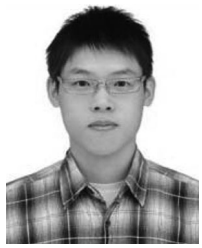

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